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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,346	09/23/2005	Kong Lim Toh	DE 030087	1325

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EXAMINER	
LEE, BENNY T	

ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
02/12/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/550,346	TOH, KONG LIM	
	Examiner	Art Unit	
	Benny Lee	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6 and 8-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,8,9; 10-16; 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 27 October 2008 has been entered.

The disclosure is objected to because of the following informalities: Note that subheadings should be provided to delineate the different portions of the specification (e.g. --Summary of the Invention--; --Brief Description of the Drawings--; etc) for clarity of description. Note that the following reference labels appearing in the indicated drawing figure still needs a corresponding specification description relative to that drawing figure: Fig. 4 (48, 50, 52, PESW). Appropriate correction is required.

Claims 1, 4-6, 8, 9; 10-16; 17-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 10, 17, note that it is unclear whether the recitation of high and low "insertion loss" between the common port and the corresponding branch port can properly apply "in each state" as recited. That is to say, the recited high and low "insertion loss" between the common port and the corresponding branch port appears to apply to only one switch state rather than "each" switch state. Clarification is needed.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

> such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 5, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heckaman et al in view of Even-or (both of record).

Heckaman et al (Fig. 6) discloses a switch circuit device comprising: two input terminals (i.e. RF IN 28, RF IN 30) and an output terminal (i.e. RF OUT 35); first switches (i.e. SPST switch modules 20, 22) having first and second ports (i.e. one port is connected to the corresponding RF IN terminal; another port is connected to corresponding transmission lines 36, 38); and a second switch (i.e. SPDT module 24) having branch ports series connected to corresponding SPST modules (20, 22) via corresponding transmission lines (36, 38). As known to those of ordinary skill in the art, an SPST (i.e. single pole-single throw) switch functions to provide either a high insertion loss (i.e. open) state or a low insertion loss (i.e. closed) state depending on the bias voltage (i.e. 5V/0V) applied to the transistors of the corresponding SPST switch (i.e. via corresponding bias voltage inputs 32, 34). In a similar manner, an SPDT (i.e. single pole-double throw) switch functions to provide either a low insertion loss (i.e. closed) state to one of the branches while providing a high insertion loss (i.e. open) state to the other one of the two branches or vice versa depending on the complementary bias voltage (i.e. 5V/0V or 0V/5V) applied to the corresponding branch (i.e. by the corresponding bias voltage applied to bias voltage inputs 32, 34). Thus the corresponding SPST switch module is electrically series connected to a corresponding branch of the SPDT module and is therefore both the SPST module and the series connected SPDT branch are biased on or off depending of the voltage applied to the corresponding bias voltage input. Regarding claim 4, it should be noted that each one of SPST switch module comprises of a plurality of "discrete electronic parts" (i.e. a plurality of

transistors". Regarding claim 5, note that Fig. 13, which is a physical realization of the switch in the fig. 6 embodiment, discloses that the switches are disposed in an "integrated circuit" configuration upon a substrate. With regard to the operation of the bias voltage being applied to the corresponding switches, note that the description at column 5, line 64 to column 6, line 2 and column 6, lines 11-21 describe how only two bias voltages or "drivers" are needed to provided the complementary (i.e. in-phase voltage signal, inverted voltage signal) bias control voltages (e.g. 5V/0V) to selectively switch the corresponding SPST & SPDT switch modules.

Note that Heckaman et al (Fig. 6) discloses the claimed invention except that the "first switches" are implemented by transistors and not by series connected PIN (i.e. switching) diodes having a driver control connected to the junction between the diodes.

However, as disclosed in an alternative realization of the switches, Heckaman et al (Fig. 3) suggests that such switches can alternatively be realized by switching PIN diodes.

Moreover, Even-or (e.g. Fig. 1A) discloses a diode switch configuration having two series connected diodes (i.e. D1, D2) connected between an input (i.e. RF_{IN}) and an output (i.e. RF_{OUT}) to thereby function in an SPST mode in response to a control signal (i.e. ON/OFF) applied to the junction (i.e. the anodes) between the diodes (D1, D2) as provided by a control driver circuit (e.g. 12, 14, 18, 20, 22), as described at column 3, lines 43-46.

Accordingly, it would have been obvious in view of the references, taken as a whole, to have modified the SPST switches in Fig. 6 in Heckaman et al with the series connected PIN diodes as taught by Even-or. Such a modification would have been considered an obvious substitution of art recognized components usable in an SPST switch, especially since Heckaman et al recognizes that PIN diodes are an equivalent type of switching element to transistors and as

such would have performed the equivalent function as the transistors within the context of the disclosed SPST switch, thereby suggesting the obviousness of alternatively using series connected diode switches in place of transistor switches.

Claims 8, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the above rejection of claims 6 & 1, respectively and further in view of Atokawa et al (of record).

As previously described, the above obviousness combination discloses the claimed SPST/SPDT switch combination, but does not disclose the use of such a switch combination in conjunction with a transceiver circuit.

Atokawa (fig. 1) discloses a transceiver circuit (i.e. transmit/receive filter 1) having two input terminals (i.e. antennas 8, 9), a tuner circuit (i.e. receive filter 3); and a switch circuit (i.e. SPDT switch (4) operatively connected to switches (6, 7) which equivalently function as SPST switches) selectively connecting the antennas (8, 9) to the tuner input (i.e. ant2).

Accordingly, it would have been obvious in view of the references, taken as a whole, to have realized the switch circuit (i.e. SPDT switch (4) in conjunction with SPST switches 6, 7) in Atokawa et al by the electrically equivalent switch in the above obviousness combination. Such a modification would have been considered an obvious substitution of art recognized equivalent switches, especially since the switch in Atokawa et al has the same electrical configuration as the switch combination set forth above, thereby suggesting the compatibility and thus the obviousness of such a modification. Moreover, as disclosed in Atokawa et al, each switch is electrically connected to a control circuit for controlling the switching state of the transceiver.

Applicant's arguments filed 27 October 2008 have been fully considered but they are not persuasive.

Regarding the inclusion of subheadings, as suggested by the examiner, it is again suggested that the inclusion of such subheadings would help delineate and thus better separate the different portions of the specification. Moreover, it is unclear in what manner the inclusion of sub-headings would affect the scope of protection afforded, as asserted by applicant. Further elaboration should be provided.

Regarding the objection for the lack of description of certain reference labels in Fig. 4, contrary to applicant's assertion, it should be noted that the various descriptions alluded to applicant at page 5 of the specification only pertain to the description of "Fig. 2" and not to the description of "Fig. 4", to which the objection in question is directed. However, in the spirit of expediting prosecution, the examiner suggests a statement indicating that like reference labels (e.g. in Fig. 4) refer to the same features described in earlier drawing figures (e.g. Fig. 2) to obviate such an objection.

Regarding the rejection of claims 1, 10, 17 on 35 USC 112, second paragraph grounds, applicant has asserted that the low "insertion loss" applies to "each" switch state and thus the claim is proper, as recited. However, it must be noted that the claim appears to improperly recite that "in each state the insertion loss between one branch port and the common port is low". That is to say, it appears that for the "one branch port", the insertion loss remains "low" for "each" switch state (i.e. switch is ON, switch is OFF), which appears contradictory to the operation of such a switch configuration (i.e. if switch is ON, insertion loss is low, if switch is OFF, insertion loss is high). Accordingly, clarification is needed. Perhaps, applicant should define the first and second switch states for the "second switch" in a manner similar to how the switch states were defined earlier for the "first switch" as a way to remedy such a deficiency.

Regarding the prior art rejection of claim 1, applicant has asserted that Heckaman et al & Even-or respectively fail to disclose "in-phase voltage signals and the inverted voltage signal are provided at the control terminal". Contrary to applicant's assertion, it should be noted that in Heckaman et al, the SPST switch module and the SPDT switch module series connected thereto operate in a complementary manner That is to say, complementary operation necessarily requires an in-phase voltage (i.e. such as 0V) and an inverted voltage (i.e. such as 5V) to selectively provide for turning on a selected one of the SPST/SPDT module, while, at the same time, selectively turning off the other one of the SPST/SPDT. Moreover, with respect to the Even-or reference, it should be noted that such a reference has been relied on primarily for recognized equivalents of anti-parallel connected diodes as being equivalent to the transistor switches in Heckaman et al, and not necessarily for the need to teach an in-phase/inverted voltage, which is already taught by Heckaman et al. Nonetheless, it should be noted that since the anti-parallel connected diodes function in substantially the same switching aspect as the transistors it replace, then it would stand to reason, a similar complementary mode of operation (i.e. in-phase/inverted voltages) would likewise have been applicable in the obvious combination. Regarding the rejection of claims 4-6, 8, 9 on prior art grounds, applicant appears to concede that these claims will rise or fall with the patentability of independent claim 1.

Any inquiry concerning this communication should be directed to Benny Lee at telephone number 571 272 1764.

/BENNY LEE/
PRIMARY EXAMINER
ART UNIT 2817

B. Lee